ABSTRACT OF THE DISCLOSURE

An apparatus and method for performing early correction of a conditional branch instruction in a pipeline microprocessor is disclosed. Early branch correction logic examines early status flags to detect a branch misprediction. The early status flags are generated in response to an instruction preceding the branch instruction earlier in the pipeline than the architected status flags are generated and may or may not be valid. If the early status flags are valid and indicate a misprediction, the early correction logic corrects the misprediction. If the pipeline stages below the early correction logic stage become void of uncompleted flag-modifying instructions, such as after a pipeline flush, the early status flags are re-validated by copying to the architected status flags to the early status flags. Late branch correction logic corrects the misprediction if the architected status flags indicate a misprediction and if the early correction logic did not correct the misprediction.